

Advanced Computer Architecture

Tutorial 9

Design Concepts in DRAM and HardDisk



NPTEL Online Course : Advanced Computer Architecture : Dr. John Jose, IIT Guwahati

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DRAM Address Mapping

- ❖ A 32 GB DRAM system that uses 4 channels (C0, C1, C2 and C3) has 4096 columns per row. It uses 8B wide memory bus to transfer data from DRAM to the processor. If adjacent memory words are mapped on to adjacent memory channels, which channel will fetch the physical address 0x 3488A742?

DRAM Address Mapping

Consider a 64 GB DRAM system organized as 4 channels, each channel with 2 DIMMs, each DIMM having 2 ranks. The system uses of 8 bit chips and **8 banks**. Each bank has a collection of byte-cells (can store 8 bit of information) organized as rows and columns. ie, the meeting point of a row and column is a byte cell. The bank configuration is in such a way that the number of rows and columns per bank is equal. The system use 8 byte wide memory bus to transfer data from DRAM to the controller. Each channel is connected to 16GB of continuous memory.

64 GB = 36 bit physical address

DRAM Address Mapping

64 GB DRAM, 4 channels, each channel with 2 DIMMs, each DIMM having 2 ranks, **8 banks**. The meeting point of a row and column is a byte cell, number of rows and columns per bank is equal. 8 byte wide memory bus to transfer data from DRAM to the controller. Each channel is connected to 16GB of continuous memory.

64 GB = 36 bit physical address

Channel	DIMM	Rank	Bank	Row	Col	Byte
2	1	1	3			3
2	1	1	3	13	13	3

DRAM Address Mapping

If the system is using row interleaving in banking, which bank the physical address 0x 844332255 is mapped to? Which channel serves data belonging to this address?

Channel	DIMM	Rank	Row	Bank	Col	Byte
2	1	1	13	3	13	3

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0x 844332255

3

0011 → Bank 3

0x 844332255

8

1000 → Channel 2

DRAM Address Mapping

If the system uses a 128B last level cache and is using cache block interleaving in banking, which bank the physical address 0x2244668AA is mapped to?

64 GB = 36 bit physical address

Cha	DIMM	Rank	Row	Col. High	Bank	Col. Low	Byte
2	1	1	13	9	3	4	3

0x 2244668AA

8AA

100010101010 → Bank 1

Row Buffer Management

- ❖ In a DRAM system that follows open row buffer management policy, which of the following sequence of commands are generated if the new request is to a different row from the row that was accessed last?
 - (A) Activate
 - (B) Precharge
 - (C) Activate followed by Precharge
 - (D) Precharge followed by Activate

Row Buffer Management

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(B) Precharge

(C) Activate followed by Precharge

(D) **Precharge followed by Activate** ✓

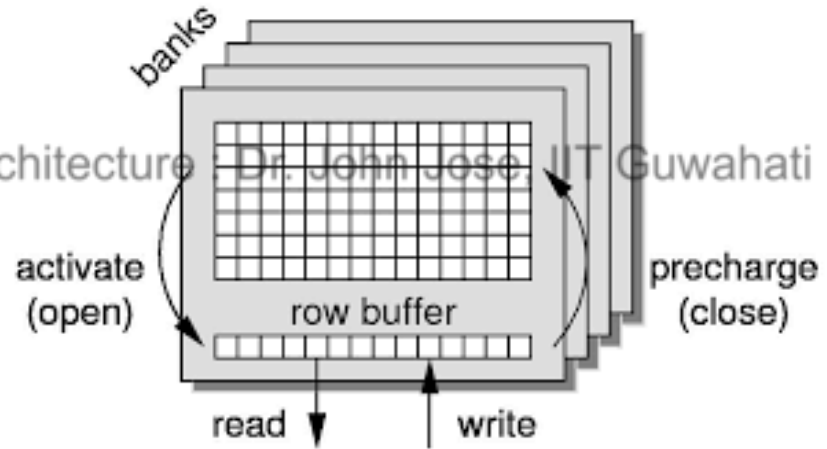
Row Buffer Management

- ❖ For a sequence of memory requests coming to a particular bank at regular intervals such that every request reaches the scheduler when the processing of the previous request is in progress, which of the following holds true for FR-FCFS scheduler?
- A. Open page policy gives lesser average turnaround time than closed page policy.
- B. Closed page policy gives lesser average turnaround time than open page policy.
- C. Closed page policy gives less average starvation than open page policy.
- D. Both open and closed page policy gives same average turnaround time.
- E. Cannot be compared with the given details.

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- C. Closed page policy gives less average starvation than open page policy.
- D. **Both open and closed page policy gives same average turnaround time.** ✓
- E. Cannot be compared with the given details.

DRAM Scheduling

A DRAM controller is using a closed page row buffer management policy. Assume that it takes 20 cycles for a row to be transferred from the storage array to row buffer after ACT is enabled, and 10 cycles for a data to be moved through data bus to memory controller after CAS is enabled. Minimum 15 cycles are needed between a PRE and an ACT signal. The controller is using FR-FCFS scheduling algorithm. Consider the following 10 memory requests that came to bank 2 of this DRAM controller. Each entry denoted by (RxCyTz) represents a request that arrived at time z^{th} clock cycle for a word at Row x and Column y of bank 2. (R15C78T10), (R20C50T20), (R24C20T35), (R20C78T80), (R2C12T150), (R24C50T180), (R35C79T200), (R10C50T210), (R24C14T220), (R25C18T250).

DRAM Scheduling

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DRAM Scheduling

Order	Time	R,C	PRE	ACT	CAS	PRE	T_C
1	10	15,78		10	30		40
	20	20,50					
	35	24,20					
	80	20,78					
	150	2,12					
	180	24, 50					
	200	35,79					
	210	10,50					
	220	24,14					
	250	25,18					

DRAM Scheduling

Order	Time	R,C	PRE	ACT	CAS	PRE	T_C
1	10	15,78		10	30		40
2	20	20,50	40	55	75		85
	35	24,20					
	80	20,78					
	150	2,12					
	180	24, 50					
	200	35,79					
	210	10,50					
	220	24,14					
	250	25,18					

DRAM Scheduling

Order	Time	R,C	PRE	ACT	CAS	PRE	T_C
1	10	15,78		10	30		40
2	20	20,50	40	55	75		85
	35	24,20					
3	80	20,78			85		95
	150	2,12					
	180	24, 50					
	200	35,79					
	210	10,50					
	220	24,14					
	250	25,18					

DRAM Scheduling

Order	Time	R,C	PRE	ACT	CAS	PRE	T_C
1	10	15,78		10	30		40
2	20	20,50	40	55	75		85
4	35	24,20	95	110	130	140	140
3	80	20,78			85		95
	150	2,12					
	180	24, 50					
	200	35,79					
	210	10,50					
	220	24,14					
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2	20	20,50	40	55	75		85
4	35	24,20	95	110	130	140	140
3	80	20,78			85		95
5	150	2,12		155	175		185
	180	24, 50					
	200	35,79					
	210	10,50					
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6	180	24, 50	185	200	220		230
	200	35,79					
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7	220	24,14			230		240
	250	25,18					

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1	10	15,78		10	30		40
2	20	20,50	40	55	75		85
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5	150	2,12		155	175		185
6	180	24, 50	185	200	220		230
8	200	35,79	240	255	275		285
	210	10,50					
7	220	24,14			230		240
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DRAM Scheduling

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9	210	10,50	285	300	320		330
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8	200	35,79	240	255	275		285
9	210	10,50	285	300	320		330
7	220	24,14			230		240
10	250	25,18	330	345	365		375

DRAM Scheduling

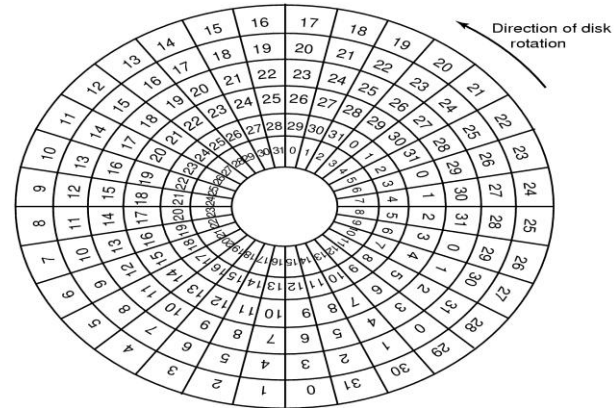
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8	200	35,79	240	255	275		285
9	210	10,50	285	300	320		330
7	220	24,14			230		240
10	250	25,18	330	345	365		375

Cylinder Skew

- ❖ If an 6000 rpm disk drive has 256 sectors per track and the track seek time is 780 μ s, what is cylinder skew?

Cylinder Skew

- ❖ Why cylinder skew?
- ❖ Offsetting the start sector of adjacent tracks to minimize the likely wait time (rotational latency) when switching tracks
- ❖ 6000 rpm disk drive rotates in 10 ms.
 - ❖ Track has 256 sectors
 - ❖ New sector every $(10/256) = 39 \mu\text{s}$
 - ❖ If track seek time $780 \mu\text{s}$
 - ❖ $780/39 \rightarrow 20$ sectors pass on seek
- ❖ Cylinder skew: 20 sectors



**THANK
YOU!**

FOR

YOUR

PRESENCE

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